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Timing-driven placement for hierarchical programmable logic devices

M Hutton, K Adibsamii, A Leaver - Proceedings of the 2001 ACM/SIGDA ninth international ..., 2001 - portal.acm.org

... **Michael Hutton**, Khosrow Adibsamii and Andrew Leaver Altera Corporation 101 ... local allows us to better **target** the true ... we need to discuss **critical path** and slack ...

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Interconnect enhancements for a high-speed PLD architecture

M Hutton, V Chan, P Kazarian, V Maruri, T Ngai, J ... - FPGA, 2002 - portal.acm.org

... **Michael Hutton**, Vinson Chan, Peter Kazarian, Victor Maruri, Tony ... delay incurred by a **critical path** is common ... The **target** density for our architecture family is ...

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Adaptive delay estimation for partitioning-driven PLD placement

M Hutton, K Adibsamii, A Leaver - IEEE Transactions on Very Large Scale Integration(VLSI) ..., 2003 - ieeexplore.ieee.org

... Given a **target** delay (constraint) on an A to B ... most stringent constraint minus the actual delay of the **path**. ... A **critical path** is one which has the minimum slack ...

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Interconnect prediction for programmable logic devices

MD Hutton - SLIP, 2001 - portal.acm.org

... wires inefficiently if it allows a more **critical** connection to have even a slightly faster **path**. ... a given design, I implemented it in the **target** device (for ...

Cited by 4 - Web Search - eecg.toronto.edu - portal.acm.org

MAX II: A Low-Cost, High-Performance LUT-Based CPLD

P Leventis, B Vest, M Hutton, D Lewis, F ... - Custom Integrated Circuits Conference, 2004. Proceedings of ..., 2004 - ieeexplore.ieee.org

... CPLD Paul Leventis*, Brad Vest, **Michael Hutton**, David Lewis ... smaller designs fall outside the **target** range of ... faster LUT inputs on the **critical path**, yielding a ...

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Characterization and parameterized generation of synthetic combinational benchmark circuits

MD Hutton, J Rose, JP Grossman, DG Corneil - IEEE Transactions on Computer-Aided Design of Integrated ..., 1998 - ieeexplore.ieee.org

... Hence, each node lies on a unique directed **path** from the ... Step A.2(a): We first consider the "**critical**" unit edges ... First, calculate **target** fanouts, **target** , ...

Cited by 14 - Web Search - ieeexplore.ieee.org - csa.com

The Quartus University Interface Program: Enabling Advanced FPGA Research

S Malhotra, TP Borer, DP Singh, SD Brown - Field-Programmable Technology, 2004. Proceedings. 2004 IEEE ..., 2004 - ieeexplore.ieee.org

... ing the final operating performance of the **target** cir- cuit ... the logic re- gion to be non-**critical** may have ... to ex- plore include the use of **path**-based approaches ...

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ACH Wu - ieeexplore.ieee.org
... gate is labeled the length of the longest **path** from any ... of a seed node (sn) to a **target** CLB (tclb ... no-connection(mc)) - E x (total wiring **delay**/no_connection(mc ...
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EMPAR: An Interactive Synthesis Environment for Hardware Emulations
TG Lee, WJ Fang, CHW Allen - Synthesis - sigda.org
... the con- straints of the **target** EM architecture ... design-quality analyzer to perform **critical delay** analysis ... Subsequent- ly, each **critical path** can be highlighted ...
View as HTML - Web Search - acm.org - ieeexplore.ieee.org

Virtual wires: overcoming pin limitations in **FPGA**-based logic emulation
JW Babb, R Tessier, A Agarwal - 1993 - lcs.mit.edu
... 7.11 Reduction Of **Critical Path** with Hybrid Wiring : : : : : 83 ... characterized by their interconnection topology network , **target FPGA** processor ...
Cited by 3 - View as HTML - Web Search - portal.acm.org - dspace.mit.edu - all 4 versions » - Library Search

Image processing PCI-based shared memory architecture design
D Houzet, A Fatni, JL Basille - The 1997 Conference on Computer Architectures for Machine ..., 1997 - doi.ieeecomputersociety.org
... This second-level ring adds a 2-cycle **delay** of latency ... to the data, according to the **target** architecture, or ... adds to the length of the **critical path** through a ...
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PC-based shared memory architecture and language
D Houzet, A Fatni - J SUPERCOMPUT, 1998 - kluweronline.com
... This second-level ring adds a 2-cycle **delay** of latency ... according to the structure of the **target** architecture. ... adds to the length of the **critical path** through a ...
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Hardware Performance Simulations of Round 2 Advanced Encryption Standard Algorithms
B Weeks, M Bean, T Rozylowicz, C Ficke - AES Candidate Conference, 2000 - mirrors.wiretapped.net
... 2.1.1 **Target** Applications ... is a function of two parameters: the worst-case **path delay** between any two ... may minimize area while another may minimize **delay** time. ...
Cited by 39 - View as HTML - Web Search - wiretapped.be - csrc.ncsl.nist.gov - csrc.nist.gov - all 13 versions »

Sigma-Dc.. Ita Modulation
ISP MAGAZINE - ieeexplore.ieee.org
... Other features such as block memory and **delay**-locked-loop technology arc also significant factors that ... This generic **FPGA** ar- chitecture is shown iii Fmg. ...
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A Stream-Based Configurable Computing Radio Testbed
S Swanchara, S Harper, P Athanas - at the IEEE Symposium on Field Programmable Custom Computing ..., 1998 - doi.ieeecs.org
... scheduled based upon the capabilities of the **target** CCM platform ... A stream is a **path** through the system that is ... the system, and is the most complex and **critical**. ...
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